COMPLEX INSTRUCTION SET COMPUTER

ABSTRACT

A computer decodes a macroinstruction to generate a number of iterations of a sequence of one or more microinstructions, including (i) a pattern of microinstructions implementing a basic operation, and (ii) a branch instruction predicted not taken. On detecting that an iteration completes operation of the macroinstruction, a marker is added to a microinstruction indicating the end of the macroinstruction in the pipeline downstream of the instruction decoder. After reaching a termination condition of the macroinstruction, an iteration beyond the termination is partially executed, the partial execution committing at least one side-effect to an architecturally-visible resource of the computer, and raising an exception to transfer control to a second microinstruction stream. In a second microinstruction stream, the side-effects committed by the post-termination iteration are unwound.